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A Verilog Design in FPGA Implementation Of Quadrature Phase Shift Keying (QPSK) Digital Modulator

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Abstract

The objective of this project deals with the design & implementation of a verilog design of QPSK Digital Modulator based on the FPGA Quartus-II simulator. Digital modulation is less complex, more secure and more efficient in long distance transmission. The noise detection and correction in digital is more efficient than analog counterpart. Digital modulation represents the transfer of the digital bit stream from the transmitter to the receiver via the analog channels. During the modulation process the information signal modifies one or more carrier parameters, leading to shift keying techniques. In past we are using analog modulation in which power, delay and area are important parameters to be considered. Hence in order to reduce power, delay and area we are using the digital modulation techniques such as BASK, BPSK and BFSK. In this paper minimum number of blocks are necessary for achieving QPSK modulation and for full integration with the other functional part of the Alter Development and Education FPGA board. The input carrier signal and the bit stream are user controllable. Hardware implemented in an FPGA can be reconfigured by programming the logic elements and interconnections for specific applications.

Keywords: BPSK, QAM, QPSK, FPGA, Verilog and Digital Modulators.

Introduction

There is a trend in communication system design and implementation to replace analogue techniques with digital techniques. This paper shows that for both voice and video, transmission coding procedures exist which result in the digitally transmitted signal occupying the same or less bandwidth than the corresponding analogue signal. Modulation is the process of conveying the information over the medium. Digital modulation represents the transfer of the digital bit stream from the transmitter to the receiver(s) via the analogue informational channel (the medium).During the modulation process the information signal modifies one or more carrier parameters. Usually, the carrier is a sine wave, defined by amplitude, frequency and phase. Depending on the carrier parameter being changed, there are three basic types of modulation techniques Binary Amplitude Shift Keying (BASK), Binary Frequency Shift Keying (BFSK) and Binary Phase Shift Keying (BPSK)[1]. All the other known modulation techniques are derived from these three basic types. The Digital Modulators often require a means to generate sinusoidal waveforms according to strong requirements regarding amplitude, phase or frequency from Electronic systems. Both the accuracy and the stability of the generated signals must usually be addressed, particularly when the parameters of interest have to be modified in real time.

Literature Survey

The research made regarding FPGAs unveiled the fact that while technology is changing, some arguments, like power consumption, that were once against the use of FPGAs, may be today their strong point. The system designer must always be up-to-date and adaptive regarding new technologies since FPGAs are going to be used more extensively in the future [2].

A literature survey shows that FPGAs are widely used in different applications, such as motor controllers [7], neural network implementations [8], finite-impulse-response (FIR) filter realization [9], fuzzy-logic controllers [10], etc. On the other hand, implementation of digital modulation and demodulation using FPGAs has received considerable attention. Signal-processing systems such as software defined radios (SDRs) can receive various kinds of modulated signals via software programming using digital signal processors (DSPs), FPGAs, general purpose processors (GPPs), and application specific integrated circuits (ASICs) [3]. In

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this context, Verilog design FPGAs are the best solution, due to their high flexibility, low cost, and high speed

Introduction Of Quadrature Amplitude Modulation[5](QAM)

Quadrature Amplitude Modulation, QAM[4], has fast become the dominant modulation mechanism for high speed digital signals. From the wireless 802.11 protocols to ADSL modems to personal communicators for the military, QAM has become a necessary part of our daily lives. With increases in processing power, QAM as a part of software defined radio (SDR) schema is now easily achievable

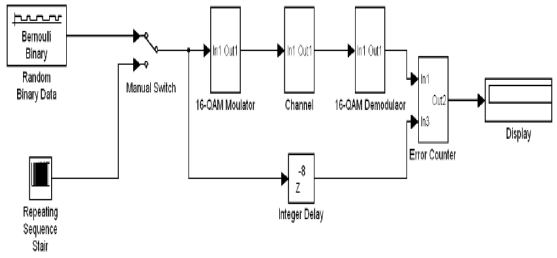

Figure 1. Block Diagram of 16 QAM Modem[5]

Quadrature Amplitude Modulation (QAM) is a modulation scheme which is carried out by changing (modulating) the amplitude of two carrier waves. The carrier waves are out of phase by 90 degrees.

Implementation Of 16-Bit QAM

The implementation has three stages Modulation, transmission, and demodulation. In our paper we discuss about only one end that is modulation involves two stages serial to parallel conversion and digital to analog conversion.

Serial to Parallel Conversion

The system must be able to modulate a serial digital input as most devices want to output data in this manner.

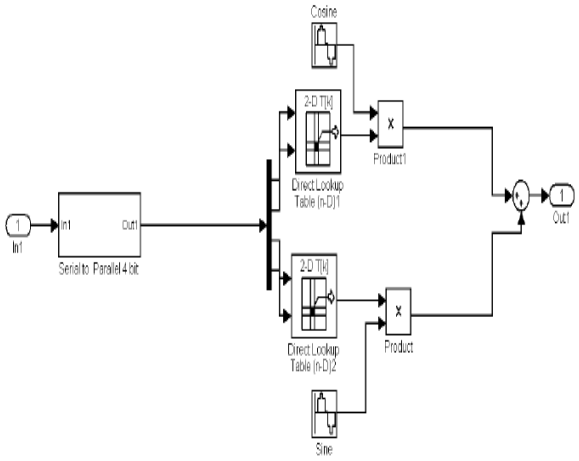

Figure 2. 16-bit QAM Modulation[5]

The first stage in the modulation block need to be a serial to parallel conversion to change the bit stream into log2*M* streams, where *M* is number of symbols in the constellation. The bit rate of each of the new streams is only 1/log2*M*.

Digital to Analog Conversion

In the case of 16-QAM there are then 4 input streams which index a lookup table. One of the simpler methods implementing the lookup table for gray coded 16-QAM uses two two-bit lookup. One of the signals then modulates the quadrature, *Q*, carrier and the other modulates the in-phase, *I*, carrier [5]. A square 16-QAM uses two amplitudes and four phases to modulate the carrier. The 4-QAM implementation uses one amplitude and four phases. For our simulated communication system the system can never become truly analog. If the sampling rate of the carrier is sufficiently greater than the symbol rate, the simulated system should approximate an analog system well. The final stage of the modulation is simply the addition of the *Q* and *I* signal to form the final M-QAM modulated signal.

Quadrature Phase Shift Keying(QPSK) Method

In QPSK, the data bits to be modulated are grouped into symbols, each containing two bits, and each symbol can take on one of four possible values: 00, 01, 10, or 11. During each symbol interval, the modulator shifts the carrier to one of four possible phases corresponding to the four possible values of the input symbol.

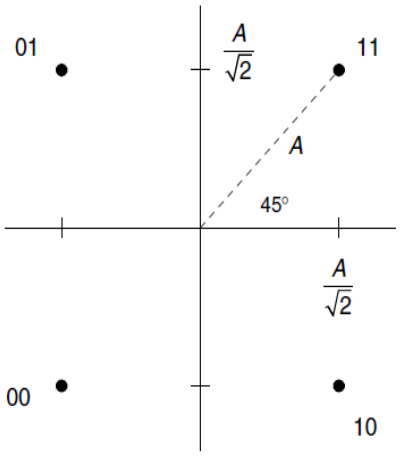

Figure 3.Ideal QPSK Constellation[5]

In the ideal case, the phases are each 90 degrees apart, and these phases are usually selected such that the signal constellation matches the configuration shown in Figure 3.

Practical QPSK modulators are often implemented using structures similar to the one shown in Figure 4.

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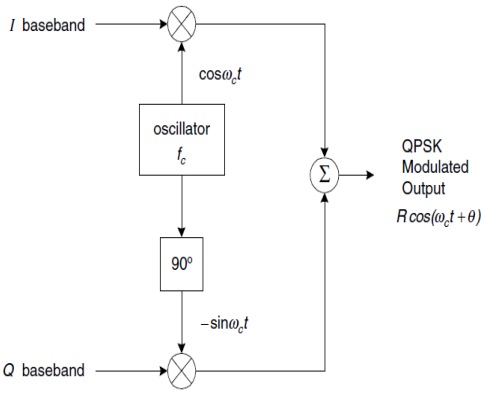

Figure 4.Block Diagram of QPSK Modulator

This structure uses the trigonometric identity
I cos ωct + Qsin ωct = R cos (ωct + θ)
Where $R = \sqrt{(I^2 + Q^2)}$
$\theta = \tan^{-1}(Q/I)$
When *I* and *Q* take on values of $\pm A/\sqrt{2}$ in all possible combinations, the phase of the resulting output signal takes on values of 45, 135, 225, and 315 degrees. If the output of this modulator is to be represented in complex-envelope form referenced to the carrier frequency, the modulated signal is given simply as
x (t) = I (t) + jQ(t)
Simulation of this idealized signal requires only a trivial model of the modulator.

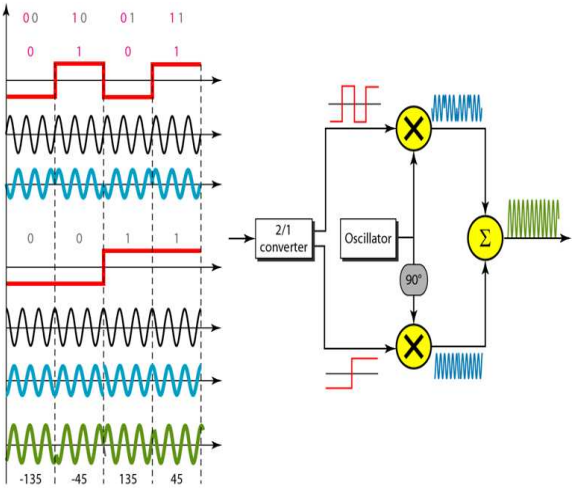

Figure 5.QPSK Block Diagram with Timing Waveforms[6]

The complex signal x (t) is formed by simply using the inphase baseband signal I (t) as the real part and the quadrature baseband signal *Q(t)* as the imaginary part.

Binary Phase Shift Keying(BPSK)

In BPSK[3], individual data bits are used to control the phase of the carrier. During each bit interval, the modulator shifts the carrier to one of two possible phases, which are 180 degrees or π radians apart. This can be accomplished very simply by using a bipolar baseband signal to modulate the carrier's amplitude, as shown in Figure 6.

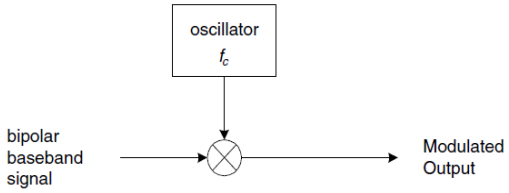

Figure 6.BPSK Modulator

The output of such a modulator can be represented mathematically as
x(t) = R(t) cos(ωct + θ)
where *R(t)* is the bipolar baseband signal, *ωc* is the carrier frequency, and θ is the phase of the unmodulated carrier. If the output of the modulator is to be represented in complex-envelope form referenced to the carrier frequency, the modulated signal is given as
x(t) = I (t) + jQ(t) …(1)
Where I (t) = R(t) cos θ
Q(t) = R(t) sin θ
In the special case of $\theta = 0$, equation 1 reduces to
x(t) = R(t)
and the real-valued baseband signal can be used directly as the complex-envelope representation of the modulator output.

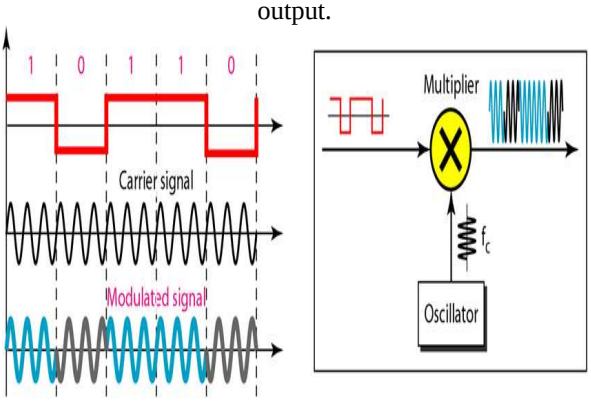

Figure 7. BPSK Block Diagram with Timing Waveforms[6]

However, to allow for subsequent phase shifting, the signal's complex-envelope representation should always be implemented as a complex-valued signal. For the special case of $\theta = 0$, the imaginary part of the complex signal is simply set to zero.

Quartus-Ii Simulation Results & Synthesis Analysis

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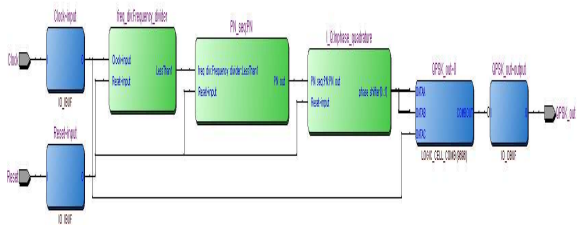

Figure 8.Technological schematic of QPSK Modulator

Frequency Divider

A frequency divider, also called a clock divider or scaler or prescaler, is a circuit that takes an input signal of a frequency, F_{in}, and generates an output signal of a frequency[11]

$F_{out} = F_{in}/n$

where n is an integer. Phase-locked loop frequency synthesizers make use of frequency dividers to generate a frequency that is a multiple of a reference frequency. Frequency dividers can be implemented for both analog and digital applications.

Flow Summary

Flow Status	Successful - Mon Jul 01 10:53:11 2013
Quartus II Version	10.1 Build 153 11/29/2010 SJ Web Edition
Revision Name	BPSK_Top
Top-level Entity Name	BPSK_Top
Family	Cyclone IV GX
Total logic elements	22 / 14,400 (< 1 %)
Total combinational functions	22 / 14,400 (< 1 %)
Dedicated logic registers	9 / 14,400 (< 1 %)
Total registers	0
Total pins	3 / 81 (4 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)
Device	EP4CGX15BF14C6
Timing Models	Final

Figure 9.Flow Summary of QPSK

The above summary gives the information about the QPSK which is simulated in Quartus II version with cyclone IV GX family in the device EP4CGX158F14C6.

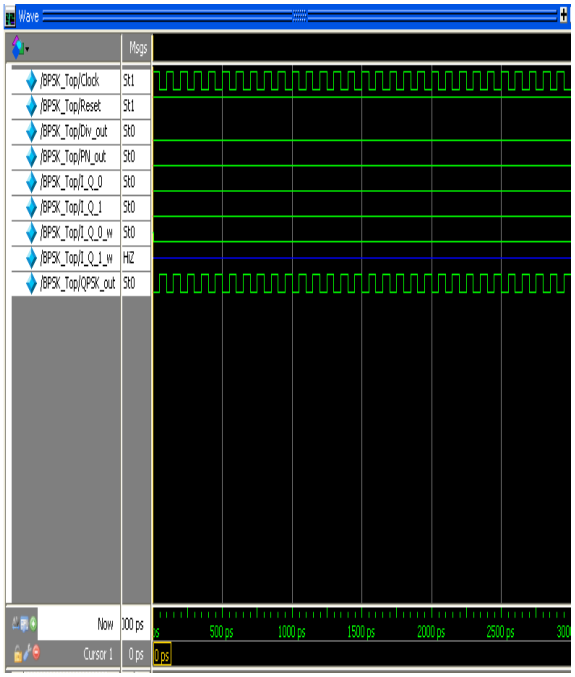

Figure 10.Simulation Result for the QPSK_Out

In the above simulated timing waveforms is obtained from Quartus II simulator which signifies the result of QPSK_OUT waveform.

PN Sequence

A pseudorandom number generator (PRNG)[11], also known as a deterministic random bit generator (DRBG), is an algorithm for generating a sequence of numbers that approximates the properties of random numbers. The sequence is not truly random in that it is completely determined by a relatively small set of initial values, called the PRNG's state, which includes a truly random seed.

Although sequences that are closer to truly random can be generated using hardware random number generators, pseudorandom numbers are important in practice for their speed in number generation and their reproducibility, and they are thus central in applications such as simulations (e.g., of physical systems with the Monte Carlo method), in cryptography, and in procedural generation. Good statistical properties are a central requirement for the output of a PRNG, and common classes of suitable algorithms include linear congruential generators, lagged Fibonacci generators, and linear feedback shift registers

The Below mentioned power play analyzer summarize that for QPSK model total thermal power dissipation is 87.44mW, Core static Thermal power dissipation is 80.89mW and IO Thermal Power dissipation is 6.55mW.

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PowerPlay Power Analyzer Summary	
PowerPlay Power Analyzer Status	Successful - Mon Jul 01 11:10:51 2013
Quartus II Version	10.1 Build 153 11/29/2010 SJ Web Edition
Revision Name	BPSK_Top
Top-level Entity Name	BPSK_Top
Family	Cyclone IV GX
Device	EP4CGX15BF14C6
Power Models	Preliminary
Total Thermal Power Dissipation	87.44 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	80.89 mW
I/O Thermal Power Dissipation	6.55 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Figure11. Power analysis of BPSK top module

In Phase Quadrature

Two periodic waveforms whose phase difference is 1/4of their output period are said to have a quadrature phase relationship. The term is also used in communication systems to describe one of the components of orthogonal decomposition.

Quadrature phase is used in a number of different applications. Rotary encoders generate two signals in quadrature phase, as this allows measurement of both distance (number of turns) as well as the direction of movement (forward or backwards).

Thermal Power Dissipation by Hierarchy

	Compilation Hierarchy Node	Total Thermal Power by Hierarchy (1)	Block Thermal Dynamic Power (1)
1	BPSK_Top	0.37 mW (0.37 mW)	0.00 mW (0.00 mW)
2	freq_div:Frequency_divider	0.00 mW (0.00 mW)	0.00 mW (0.00 mW)
3	I_Q:Inphase_quadrature	0.00 mW (0.00 mW)	0.00 mW (0.00 mW)
4	PN_seq:PN	0.00 mW (0.00 mW)	0.00 mW (0.00 mW)
5	hard_block:auto_generated_inst	0.00 mW (0.00 mW)	0.00 mW (0.00 mW)

Figure 12.Thermal power dissipation by the Basic Building Blocks

Conclusions

In FPGA implementation we use intellectual property. The simplicity of construction was reached using intellectual property component in a combination with the HDL language. FPGA implementations of BPSK, and QPSK digital modulators are demonstrated. The main advantage of the implementations is the minimum numbers of digital blocks used for performing digital modulations, the ability to integrate with modules in FPGA boards, and the user controllability of the input signal's frequencies.

Implementation of Conventional BPSK modulation is shown in the Figure13. In this design Binary pattern and carrier frequency is variable.

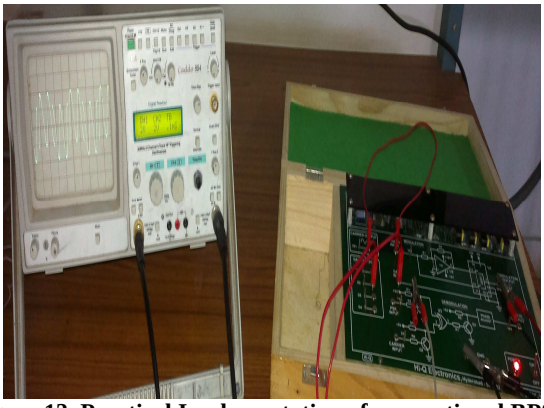

Figure 13. Practical Implementation of conventional BPSK modulation output

In addition, comparison to different performance parameters of modulation techniques will be analyzed. The implemented FPGA designs are suitable for realization of the digital baseband-modulation part of software-defined radio systems. In addition, usage of this kind of implementation for educational purposes in digital communications laboratories or courses clearly emphasizes the correlation between different courses in electronics engineering.

The simulation results show that the design principles are correct and effective. After synthesizing the system we got the statistical data about the number of input-output buffers, the number of registers, and logic elements used in the usage of Quartus II FPGA tool. These results show that the utilization of the device resources is quite minimal.

Acknowledgements

It is a pleasure to recognize the many individuals who have helped me in completing this technical paper. I sincerely express heartiest thanks to my Project guide **Sri S.Mohan Das garu** who contributed the technical guidance and encouragement and also Valuable suggestions & inspirations from HOD of ECE **Sri M.Mahaboob Basha garu**.

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